**DSD Semester Projects List**

1. Implementation of MIPS Processer (R&I-type instructions) in Verilog HDL.
2. Implementation of 32-bit signed multiplier in Verilog HDL. (Conventional method)
3. 10th Order FIR filter
4. Convolutional Encoder
5. REED SOLOMON ENCODER
6. Traffic Light Controller
7. USART
8. RISC Processor
9. Barrel Shifter

Important deadlines: Project proposal> 12th December 2022

Project Final Demo: Lab Final